Amendments to the Abstract

Please replace the paragraph at page 34, lines 6 through 14 with the following amended paragraph:

The present invention generally provides a packet buffer random access memory (PBRAM) device including a memory array, a plurality of input ports, and a plurality of serial registers associated with the input ports. ~~that is optimized for network packet switching. Multiple access~~ The plurality of input ports permit multiple devices to concurrently access the memory in a non-blocking manner. The serial registers enable receiving data from the input ports and concurrently packet data to the memory array. The memory performs all management of network data queues so that all port requests can be satisfied within the real-time constraints of network packet switching. ~~The memory system is expandable, with packet data being distributed across all memories in the system to prevent overloading of any one memory device. Further, the memory system includes input and output queue management functions using pointers that allow input data to be placed on output data queues without the data actually being copied into a new output queue.~~